REMARKS

Claims 1 - 35, 37, 38 and 42 - 45 are pending in the above-identified application. Claims 1 - 19 are withdrawn from consideration.

In the Office Action of November 20, 2002, Claims 20 - 35, 37, 38 and 42 - 45 were rejected. No claim was allowed. In response, Claims 20, 25, 26 and 29 - 31 are amended and Claims 24 and 28 are canceled. Reexamination and reconsideration are respectfully requested in view of the foregoing amendments and the following remarks.

The Invention

The invention as set forth in the amended claims is a method of fabricating a semiconductor integrated circuit device having damascene type interconnections with thin conducting barrier films and pure copper wiring, where a chemical mechanical polishing (CMP) process is performed using a polishing slurry containing an oxidizing agent of copper and organic acid capable of dissolving an oxide of copper within a corrosion region of copper. Claim 20 is amended to incorporate the limitations of Claims 24 and 28 that an abrasive-free polishing slurry is used to reduce damage during the CMP process, and a reducing plasma treatment is performed after the CMP to remove any remaining damage.

Rejection of Claims 20, 28 - 35, 37 - 38 and 42 - 45 under 35 U.S.C. §103(a) over Edelstein in view of Nogami

Claims 20, 28 - 35, 37 - 38 and 42 - 45 are rejected under 35 U.S.C. §103(a) as being obvious over Edelstein et al (U.S. Patent No. 6,181,012) in view of Nogami

et al (U.S. Patent No. 6,242,349). The Examiner alleges that Edeistein discloses a method of fabricating a semiconductor integrated circuit device comprising, providing a semiconductor substrate (52) having a first main surface, forming a first insulating film (54) over the first main surface of the semiconductor substrate, forming an embedded interconnection slot over the first insulating film main surface, forming a connecting hole in a bottom surface of the embedded interconnection slot, and connected to a lower conducting layer (46), forming a conducting barrier film (72) over surface region of the bottom surface and side surface of the embedded interconnection slot and the connecting hole, forming an embedded metal interconnection layer (56) having copper as its main component embedded in the interconnection slot and in the connecting hole in which the conducting barrier film is formed, forming a cap insulating film (silicon nitride, 101) so as to cover the embedded metal interconnection layer and the upper surface of the first insulating film, wherein, the concentration of components other than copper in the embedded metal interconnection layer in the finished semiconductor integrated circuit device does not exceed 0.8At% (0.001 wt% C), and the film thickness of the thinnest part of the conducting barrier film in the side walls of the embedded interconnection slot and the connecting hole is about 10nm. The Examiner acknowledges that Edelstein does not disclose that the thickness of the conducting barrier film is less than 10nm. The Examiner alleges that Nogami discloses an integrated circuit device having the conducting barrier film with the thickness between 5 nm to about 150 nm. The Examiner takes the position that it would have been obvious to form the conducting barrier film of Edelstein having a thickness of less then 10nm, such as taught by

Nogami in order to reduce the contact resistance and to improve the circuit performance.

Regardng Claim 28, the Examiner alleges that Edelstein and Nogami disclose performing the CMP to the first metal film. The Examiner takes the position that it would have been obvious to perform the abrasive particle-free CMP in order to prevent the surface damage to the first insulating film.

Regarding Claims 29-31, the Examiner takes the position that although Edelstein and Nogami do not teach the exact mass ratio of abrasive particles, it would have been obvious to form the circuit having the desired mass ratio of abrasive particles as involving only routine skill in the art.

Regarding Claim 37, the Examiner alleges that Edelstein and Nogami disclose that the film thickness of the thinnest part of the conducting barrier film in the side walls of the embedded interconnection slot and the connecting hole is not more than 5nm.

Regarding Claims 38 and 42, the Examiner alleges that Edelstein and Nogami disclose that there might be no conducting barrier film.

Regarding Claims 43-45, the Examiner alleges that Edelstein and Nogami disclose that the width of the embedded interconnection slot does not exceed 0.4 μm (less than 0.5 μm).

This rejection is respectfully traversed as it may apply to the amended claims. In particular, independent Claim 20 is amended to incorporate the limitations of Claims 24 and 28. The present invention includes a step of chemical mechanical polishing using a polishing slurry having the property of being in the corrosion region of copper. As explained in the specification, for example on page 75, (paragraph

[0262] of the substitute specification) this feature of the present invention allows for an abrasive-free slurry to be used so that chemical mechanical process can be carried out with minimal damage. Edelstein and Nogami do not teach or suggest a polishing slurry having the property of being in the corrosion region of copper. Contrary to the Examiner's allegation that it would be obvious to provide an abrasive-free slurry, without a teaching of a polishing slurry in the corrosion region of copper, Edelstein and Nogami provide no guidance for obtaining an abrasive-free slurry that would be effective for chemical mechanical polishing.

Accordingly, it is respectfully submitted Claims 20, 29 - 35, 37 - 38 and 42 - 45 are not anticipated by or obvious over Edelstein and Nogami, alone or in combination.

Rejection of Claims 21 - 23 under 35 U.S.C. §103(a) over Edelstein in view of Nogami and further in view of Maekawa

Claims 21 - 23 are rejected under 35 U.S.C. §103(a) as being obvious over Edelstein and Nogami and further in view of Maikawa (U.S. Patent No. 6,171,957). The Examiner alleges that Edelstein and Nogami disclose all of the claimed limitations except that the metal film is formed by sputtering using a target wherein the purity of copper is not less than 99.999%. The Examiner alleges that Maekawa discloses forming a metal film by sputtering using a target wherein the purity of copper is not less than 99.999%. The Examiner takes the position that it would have been obvious to form the metal film of Edeistein and Nogami by sputtering using a target wherein the purity of copper is not less than 99.999%, such as taught by Maekawa in order to reduce the resistance of the metal film.

Regarding claims 21 and 23, The Examiner alleges that Edelstein, Nogami and Maekawa disclose copper having purity of 99.999 wt% or higher. The Examiner acknowledges that Edelstein, Nogami and Maekawa do not disclose copper having purity of 99.9999 wt%. The Examiner takes the position that it would have been obvious to form the copper having purity of 99.9999 wt% in order to produce the small line width and to increase the speed of the device to meet the performance goal.

This rejection is respectfully traversed as it may apply to the amended claims. As discussed above, the present invention includes a step of chemical mechanical polishing using a polishing slurry having the property of being in the corrosion region of copper. Neither Edelstein, Nogami nor Maekawa teach or suggest the use of a polishing slurry having the property of being in the corrosion region of copper.

Accordingly, it is respectfully submitted Claims 21 - 23 would not have been obvious over Edelstein, Nogami, and Maekawa, alone or in combination.

Rejection of Claims 24 - 27 under 35 U.S.C. §103(a) over Edelstein in view of Nogami and further in view of Lai

Claims 24 - 27 are rejected under 35 U.S.C. §103(a) as being obvious over Edelstein in view of Nogami and further in view of Lai (U.S. Patent No. 6,136,680). The Examiner alleges that Edelstein and Nogami disclose that metal film is planarized by chemical mechanical polishing. The Examiner acknowledges that Edelstein and Nogami do not disclose that the first main surface of the semiconductor substrate is plasma treated in an atmosphere of a gas having reducing properties prior to forming a cap insulating film. The Examiner alleges that

Lai discloses forming a metal film that is planarized by chemical mechanical polishing and that a first main surface of the semiconductor substrate is plasma treated in an atmosphere of a gas having reducing properties prior to forming a cap insulating film. The Examiner takes the position that it would have been obvious to plasma treat the first main surface of the semiconductor substrate of Edeistein and Nogami in an atmosphere of a gas having reducing properties prior to forming a cap insulating film in order to suppress hillocks formation.

Regarding claims 25-27, the Examiner alleges that Edelstein, Nogami and Lai disclose that the gas atmosphere comprises hydrogen (ammonia) and/or nitride hydride as its principal component element.

This rejection is respectfully traversed as it may apply to the amended claims. In particular, the rejection is traversed as it may be applied to Claim 20, which now contains the limitations of canceled Claim 24. As discussed above, the present invention includes a step of chemical mechanical polishing using a polishing slurry having the property of being in the corrosion region of copper. As discussed above, neither Edelstein nor Nogami teach or suggest the use of a polishing slurry having the property of being in the corrosion region of copper. Likewise, Lai does not teach the use of such a polishing composition as an abrasive-free polishing slurry.

Accordingly, it is respectfully submitted Claim 20, and claims depending thereon, would not have been obvious over Edelstein, Nogami and Lai, alone or in combination.

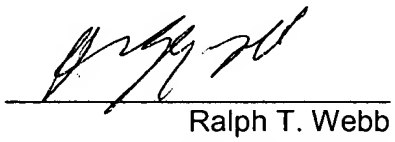
Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that Claims 20 - 23, 25 - 27, 29 - 35, 37 - 38 and 42 - 45 are in condition for allowance. Favorable reconsideration is respectfully requested.

Should the Examiner believe that anything further is necessary to place this application in condition for allowance, the Examiner is requested to contact applicants' undersigned attorney at the telephone number listed below.

Kindly charge any additional fees due, or credit overpayment of fees, to Deposit Account No. 01-2135 (501.39932X00).

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS



Ralph T. Webb
Reg. No. 33,047

RTW/RTW
(703)312-6600

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IN THE CLAIMS

20. (twice amended) A method of fabricating a semiconductor integrated circuit device comprising:

(a) providing a semiconductor substrate having a first main surface,

(b) forming a first insulating film over said first main surface of said semiconductor substrate,

(c) forming an embedded interconnection slot ~~over~~ in said first insulating film over the main surface,

(d) forming a connecting hole in a bottom surface of said embedded interconnection slot~~, and~~ connected to a lower conducting layer,

(e) forming a conducting barrier film over a surface region of the first insulating film outside said embedded interconnection slot and said connecting hole and the bottom surface and side surface of said embedded interconnection slot and said connecting hole,

(f) forming a metal film having copper as its main component over the conducting barrier film so as to fill said embedded interconnection slot and said connecting hole,

~~(f)~~ (g) removing the metal film outside said embedded interconnection slot and said connecting hole by a chemical mechanical polishing method using a polishing slurry containing an oxidizing agent of copper and organic acid capable of dissolving an oxide of copper within a corrosion region of copper, thereby forming an

embedded metal interconnection layer having copper as its main component embedded in said interconnection slot and in said connecting hole in which said conducting barrier film is formed, ~~and~~

(h) performing plasma treatment to the surface region of the first insulating film and a surface of the embedded metal interconnection layer in a gas atmosphere having reducing properties; and

~~(g)~~ (i) after step (h), forming a cap insulating film so as to cover said embedded metal interconnection layer and the upper surface of said first insulating film, wherein:

the concentration of components other than copper in said embedded metal interconnection layer in the finished semiconductor integrated circuit device does not exceed 0.8At%, and

the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is less than 10 nm.

25. (amended) A method of fabricating a semiconductor integrated circuit device as defined in Claim ~~24~~ 20, wherein said gas atmosphere comprises hydrogen as its principal component element.

26. (amended) A method of fabricating a semiconductor integrated circuit device as defined in Claim ~~24~~ 20, wherein said gas atmosphere also has a nitriding action.

29. (amended) A method of fabricating a semiconductor integrated circuit device as defined in Claim ~~28~~ 20, wherein the proportion of abrasive particles in ~~a~~ the polishing slurry ~~used for said abrasive particle-free chemical mechanical polishing,~~ does not exceed 0.5% as a mass ratio.

30. (amended) A method of fabricating a semiconductor integrated circuit device as defined in Claim ~~28~~ 20, wherein the proportion of abrasive particles in ~~a~~ the polishing slurry ~~used for said abrasive particle-free chemical mechanical polishing,~~ does not exceed 0.1% as a mass ratio.

31. (amended) A method of fabricating a semiconductor integrated circuit device as defined in Claim ~~28~~ 20, wherein the proportion of abrasive particles in ~~a~~ the polishing slurry ~~used for said abrasive particle-free chemical mechanical polishing,~~ does not exceed 0.05% as a mass ratio.

(f) an embedded metal interconnection layer having copper as its main component embedded in said interconnection slot and in said connecting hole in which said conducting barrier film is formed, and

(g) a cap insulating film formed so as to cover said embedded metal interconnection layer and the upper surface of said first insulating film, wherein:

the concentration of components other than copper in said embedded metal interconnection layer in the finished semiconductor chip does not exceed 0.8At%, and

the purity of copper in the metal film when an embedded metal film having copper as its principal component is formed to form said embedded metal interconnection layer, is not less than 99.999%.

21. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the purity of said copper is not less than 99.9999%.

22. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein said metal film is formed by sputtering using a target wherein the purity of copper is not less than 99.999%.

23. A method of fabricating a semiconductor integrated circuit device as defined in Claim 21, wherein said metal

film is formed by sputtering using a target wherein the purity of copper is not less than 99.9999%.

24. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein said metal film is first planarized by chemical mechanical polishing, and said first main surface of said semiconductor substrate is plasma treated in an atmosphere of a gas having reducing properties prior to forming said cap insulating film.

25. A method of fabricating a semiconductor integrated circuit device as defined in Claim 24, wherein said gas atmosphere comprises hydrogen as its principal component element.

26. A method of fabricating a semiconductor integrated circuit device as defined in Claim 24, wherein said gas atmosphere also has a nitriding action.

27. A method of fabricating a semiconductor integrated circuit device as defined in Claim 26, wherein said gas atmosphere comprises ammonia as its principal component element.

28. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein said chemical

mechanical polishing for forming the embedded metal interconnection layer is performed by abrasive particle-free chemical mechanical polishing.

29. A method of fabricating a semiconductor integrated circuit device as defined in Claim 28, wherein the proportion of abrasive particles in a slurry used for said abrasive particle-free chemical mechanical polishing, does not exceed 0.5% as a mass ratio.

30. A method of fabricating a semiconductor integrated circuit device as defined in Claim 28, wherein the proportion of abrasive particles in a slurry used for said abrasive particle-free chemical mechanical polishing, does not exceed 0.1% as a mass ratio.

31. A method of fabricating a semiconductor integrated circuit device as defined in Claim 28, wherein the proportion of abrasive particles in a slurry used for said abrasive particle-free chemical mechanical polishing, does not exceed 0.05% as a mass ratio.

32. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the concentration of components other than copper does not exceed 0.2At%.

33. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the concentration of components other than copper does not exceed 0.08At%.

34. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the concentration of components other than copper does not exceed 0.05At%.

35. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the concentration of components other than copper does not exceed 0.02At%.

36. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is less than 10nm.

37. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thinnest part of said conducting barrier

film in the side walls of said embedded interconnection slot and said connecting hole is not more than 5nm.

38. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 3nm.

39. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is less than 10nm.

40. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 5nm.

41. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20 wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 3nm.

42. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 2nm, or there is no conducting barrier film.

43. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the width of said embedded interconnection slot does not exceed 0.4μm.

44. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the width of said embedded interconnection slot does not exceed 0.25μm.

45. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the width of said embedded interconnection slot does not exceed 0.2μm.